REMARKS

Claims 1-44 were pending, with claims 10 and 39 objected to and the remainder rejected. Claims 1, 6-9, 12-15, 18-20, 24, 27-30, 32, and 35-44 are amended herein, and claims 16, 17, 25, 26, 33, and 34 are canceled. Accordingly, claims 1-15, 18-24, 27-32, and 36-44 remain active in the application. Reconsideration and allowance of the present application is respectfully requested in light of the claim amendments and the following remarks.

Response to Rejections

Rejections Based on Wynne alone or in combination with Tran or Stallings

Original claims 1-4, 6, 7, 11, 15-17, 19, 22-27, 29, 32-38, 41 and 42 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wynne (U.S. Pat. App. 2003/0016686 A1). Claims 5, 12, 14, 20, 30, 43 and 44 were similarly rejected under 35 U.S.C. § 103(a) as being unpatentable over Wynne in view of Tran (U.S. Pat. App. 2003/0084246 A1). Claims 21 and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wynne in view of "Data and Computer Communications" to William Stallings. Applicants respectfully traverse these rejections on the grounds that Wynne and Tran are not prior art to the instant application.

Wynne and Tran are published U.S. Patent Applications with a publication date after Applicants' filing date, and a filing date of July 18, 2001, prior to Applicants' November 16, 2001, filing date. Wynne and Tran are therefore presented as prior art under the provisions of 35 U.S.C. §102(e).

Applicant submitted, along with the response to the September 21, 2005, Office Action, a declaration under the provisions of 37 C.F.R. § 1.131. The Examiner stated in the March 8, 2006 Final Office Action that the declaration was ineffective to remove Wynne and Tran as references, and supplied a list of what the Examiner regarded as deficiencies in the declaration. Applicant argued against these deficiencies. In the Advisory Action of June 28, 2006, the Examiner agreed to withdraw all but the sixth and seventh objections. On August 2, 2006, Applicant filed a Request for Continued Examination and a second inventor declaration under the provisions of 37 C.F.R. § 1.131 that further clarified the functionality of the device reduced to practice. The Examiner maintains that certain claim limitations are not established by the declarations, and therefore the declarations are insufficient to overcome the rejections.

With reference to the second declaration, the Examiner states that it is "unclear from the factual evidence provided that the Cheetah is 'an input for receiving packets, each packet associated with an output queue' (or equivalent) as recited in the claims." (October 3, 2006 Office Action at 3). First, as stated in ¶ 6 of Mr. Chung's declaration, the Cheetah is not the buffer manager or any portion thereof, but is a separate ASIC for maintaining and searching forwarding databases. The Cheetah's inclusion in the affidavit merely explains where the Tiger ASIC obtains the output queue assignment for each packet. Mr. Chung states "the forwarding lookup allowed the Tiger to send the Cougar ASIC packets containing an 'F10 header'—a proprietary header that was prepended to each packet prior to passing the packet to the Cougar." (Heeloo Chung 2nd Decl., ¶ 6.) The input for receiving packets is clearly shown on page 1 of Exhibit A, as a "Front End C-Port Interface" in the "data path" from "Tiger." This description is entirely consistent with the patent application description of a lookup engine and C-port blocks that include the physical input ports for the buffer manager, including the description:

> By the time the packets have entered the C-port block 110, they have already been assigned to a particular VOQ by the lookup engine 40 (FIG. 1). The VOQ to which the packet is assigned, as well as other data and commands are present in a header of each packet. (Application, p. 4, l. 31 to p. 5, l. 8.)

The Examiner also states that "the information provided on pages 16-17 of Exhibit A show packet header information for a Cougar interface but makes no reference that the packet header format is an 'F10 header' as taught by the rest of the Exhibit." (October 3, 2006 Office Action at 3). This objection appears irrelevant, as the inventor and author of Exhibit A has stated that the F10 ("Force10") header is the proprietary header described (see ¶ 7), and this fact is sufficient to equate the two under USPTO guidance:

> However, when reviewing a 37 CFR 1.131 affidavit or declaration, the examiner must consider all of the evidence presented in its entirety, including the affidavits or declarations and all accompanying exhibits, records and "notes." An accompanying exhibit need not support all claimed limitations, provided that any missing limitation is supported by the declaration itself. M.P.E.P. § 715.07.I.

Applicant respectfully requests that the Examiner consider the evidence presented in its entirety, including the inventor declaration—this evidence establishes that at the Cougar packet input a header is received with each packet, and the header identifies an output queue association.

The Examiner further states that he "found no evidence that Exhibit A teaches at least an intermediate storage facility manager configured to assign particular block of the intermediate storage facility to output queues, and store one or more packets associated with output queues into blocks assigned to those output queues." (October 3, 2006 Office Action at 3). "In particular, there is no further description with respect to the figure shown on page 12 of the exhibit. Thus it is unclear that 'p1a' is a part 'a' of a 'packet 1' as argued by applicant." (*Id.* at 4). A description of the example page 12 figure is, however, provided in the declaration, including the description of the packet labeling. This is part of the evidence, not an argument by the applicant, and must be considered as evidence according to the USPTO guidance. The evidence establishes that the Cougar ASIC included the intermediate storage facility manager.

Rejections Based on Wilford

Original claims 1-9, 11-28, and 40-44 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wilford (U.S. Pat. 6,687,247 B1). Applicant respectfully traverses this rejection on the grounds that Wilford fails to disclose all elements of any rejected claim.

Applicant has amended the claims of the application to make explicit what is implied by the original claim language. For instance, claim 1 recited an intermediate storage facility and manager to assign particular blocks of the intermediate storage facility to output queues. Applicant has amended this language to make explicit the block assignment—"to assign particular blocks of the intermediate storage facility to buffer packet data according to destination output queues," thus leaving no question that the intermediate storage facility is not the output queues but intermediate storage as packet data moves toward the output queues. Dependent claims 6-9 and 12-14 have been amended to make explicit that the "second storage facility" is the queue memory.

Independent claims 15, 24, and 32 have been amended using, e.g., concepts from now-canceled dependent claims 16, 17, 25, 26, 33, and 34. Claims 15, 24, and 32 now recite the sorting of packet data into groups having common assigned output queues for storage in the buffer memory, and block storage memory to received the grouped packet data.

Independent method claim 35 has been amended to make explicit that the packet data aligned within each group has a common output queue, and that the packet data groups are buffered in the blocks of a memory buffer prior to selection for storage in a memory device

comprising the output queues. The remaining dependent claims have been amended to provide consistency with amended claim 35. No new matter has been added by the amendments.

Regarding the Wilford rejection, with respect to claim 1, that claim is patentable over Wilford at least because Wilford fails to teach "an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility to buffer packet data according to destination output queues, and store one or more packets associated with the output queues into the blocks assigned to those output queues." The rejection appears to read Wilford's queue memory as the intermediate storage facility. This reading is incorrect, as is further accentuated by the amendment that makes explicit the limitation wherein the intermediate storage facility buffers packet data according to destination output queues. Wilford uses a simple cell FIFO as an intermediate storage facility, and thus does not assign particular blocks according to destination output queues as claimed:

> Packets that pass the RED test are segmented into 64 byte cells and written into an Input Cell FIFO. This 32 Kbit buffer provides some smoothing between the input stream and the DRAM write operations which are not deterministic...Cells are dequeued from the Input Cell FIFO and written into DRAM to the appropriate output queue. (Wilford, col. 31, ll. 25-36.)

Regarding the additional limitations found in the dependent claims of claim 1, the rejection generally points to functions of Wilford's output queue and queue manager, and not to functions of an intermediate storage facility and facility manager as claimed. Further, with respect to claim 9, Applicant did not understand the rejection "see, e.g., CAR which uses tokens" and how the rejection applies to teachings found in Wilford.

Regarding claim 15, that claim is patentable over Wilford at least because Wilford fails to teach a buffer memory and buffer memory manager as claimed. As noted above, Wilford uses an Input Cell FIFO to store packet cells prior to writing to DRAM queues, not a buffer memory having blocks of storage locations as claimed. As Wilford's Input Cell FIFO is merely a FIFO, no manager for the FIFO is used.

Regarding the additional limitations found in the dependent claims of claim 15, the rejection generally points to functions of Wilford's output queue and queue manager, and not to functions of a buffer memory and buffer memory manager that operate prior to output queueing.

Claims 24 and 27-32 are patentable over Wilford at least for the reasons presented above for the patentability of claim 15 and its dependent claims.

Claim 35 is patentable over Wilford at least because Wilford fails to teach aligning data packets into groups of packet data, each group comprising packet data having the same output queue, buffering the packet data groups in the blocks of a memory buffer arranged by blocks, and selecting buffered packet data groups for storage in a memory device comprising the output queues. As described above, Wilford stores packets in an Input Cell FIFO as received, with no alignment into packet data groups and buffering the groups for storage in output queues. Regarding the additional limitations found in the dependent claims of claim 35, the rejection generally points to functions of Wilford's output queue and queue manager or other unrelated switch functions, and not to functions performed during buffering prior to writing to output queues.

Rejections Based on Barri

Original claims 1, 15, 24, 32, and 35 were rejected under 35 U.S.C. § 102(e) as being anticipated by Barri (U.S. Pat. 6,757,795 B2). Applicant respectfully traverses this rejection on the grounds that Barri fails to disclose all elements of any rejected claim. Furthermore, although Applicant has not at this point gone to the expense of procuring yet another inventor declaration, Applicant does not concede that Barri is prior art to the instant application based on the claimed April 3, 2001 priority date. Should the Examiner disagree that the amended claims are clearly patentable over Barri, Applicant may elect to traverse the application on grounds that Barri is not prior art.

The Examiner alleges that the intermediate storage facility is taught as the DRAM memory system 21 shown in Figure 1B. Barri Figure 3 and the accompanying text refers to a structure and method for reading out of DRAM memory 51, not into the DRAM memory, and thus Applicant fails to appreciate how the elements of Figure 3 can possibly relate to the elements of the rejected claims as proposed in the rejection.

It is also not clear from the rejection that Barri receives at the input packets associated with output queues, and Applicant could not locate this element in Barri. Further, in Barri, it is clear that no intermediate storage facility or facility manager is disclosed. With reference to Figure 1B, "receiver controller 22 receives data from incoming bus labeled Data_in and issues write requests in order to write receive data into individual buffers in memory system 21." (Barri, col. 4, ll. 52-55). Thus even if the memory system 21 includes output queues (a teaching that Applicant has been unable to locate in Barri), according to Barri the receiver controller 22

merely writes received data to the memory system in the order received, like Wilford above, and fails to buffer packet data according to destination output queues within an intermediate storage facility as claimed.

A similar analysis following along the lines given above for Wilford is applicable to the remaining independent claims.

Accordingly, Applicant respectfully requests that the rejection based on Barri be withdrawn.

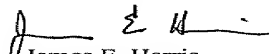
Response to Objections

Claims 10 and 39 were pending and were objected to as being dependent upon a rejected base claim. For the aforementioned reasons, the base claims from which claims 10 and 39 depend are patentable over the art of record. Applicants respectfully request that the instant objections be withdrawn.

Conclusion

For the foregoing reasons, Applicants respectfully request allowance of claims 1-15, 18-24, 27-32, and 36-44 as presently constituted. The Examiner is encouraged to telephone the undersigned at 512.867.8502 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,



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